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EXAMINER	
SORRELL, ERON J	
ART UNIT	**PAPER NUMBER**
2182	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,321	HUSSAIN ET AL.	
	Examiner	Art Unit	
	Eron J Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 23-36* is/are rejected.

7)☒ Claim(s) *17-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 15,16, 23-30, 32-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Petersen (U.S. Patent No. 5,517,627).

3. Referring to claim 15, Petersen teaches a method of performing a fly-by read operation, the method comprising the steps of:

reading data words from a memory device in a slave peripheral, wherein the each of the data words includes N bytes (see lines 16-37 of column 12);

incrementing a read pointer of the memory device each time a data word is read from the memory device (see lines 12-13 of column 13 and lines 47-50 of column 13; Note the queue count value is the read pointer);

aligning the data words read from the memory device to a system bus (see lines 16-37 of column 12); and

adjusting the read pointer at the end of the fly-by read operation (see lines 12-13 of column 13 and lines 47-50 of column 13; Note the Examiner is relying on the definition of fly-by transactions found in paragraph 2 of page 1 of the applicant's specification).

4. Referring to claim 16, Petersen teaches the method further comprises the step of providing byte enable signals on the system bus using a direct memory access (DMA) controller, the byte enable signals corresponding with bytes of data words being transferred (see lines 17-37 of column 12).

5. Referring to claim 23 and 32, Petersen discloses operating the memory device in a first in, first out (FIFO) manner (see lines 17-23 of column 12).

6. Referring to claims 24 and 25, Petersen teaches a method of performing fly-by write operation between a memory device and a slave device comprising:

reading the first data word from the memory device, wherein the first data word is not aligned with the system bus, such

that the first data word includes a first set of one or more bytes included in the fly-by write operation, and a second set of one or more bytes to be excluded from the fly-by write operation (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5);

transmitting an invalid data word on the system by to a slave device, wherein the invalid data word includes the second set of one or more bytes of the first data word (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5);

transmitting a disabling byte enable on the system bus to a slave device, the disabling byte-enable value corresponding with the invalid data word and coming from the DMA controller (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5);

preventing the invalid data word from being written to the slave device in response o the disabling byte-enable value (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5).

7. Referring to claim 26, Petersen teaches the method further comprises:

providing a first address signal from the DMA controller to the memory device (see paragraph bridging columns 9 and 10);

retrieving the first data value from the memory device in response to the first address signal (see paragraph bridging columns 9 and 10).

8. Referring to claim 27, Petersen teaches the method further comprising:

reading a second data word from the memory device, wherein the second data word is not aligned with the system bus (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5)l

transmitting the first fly-by write data word on the system bus to the slave device (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5);

transmitting a first byte-enable word on the system bus to the slave device, the first byte enable word corresponding with the first fly-by write data word (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5);

writing the first fly-by write data word to the slave device in response to the first byte-enable word (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5).

9. Referring to claims 28, Petersen discloses the method comprises shifting the fly-by write data word in the slave device in response to an alignment signal (see lines 40-55 of column 10).

10. Referring to claim 29 and 30, Petersen teaches providing an alignment signal that identifies a degree of misalignment between the first data word on the system bus (see lines 40-67 of column 10 and column 11 and lines 1-15 of column 12); and

combining the first set of one or more bytes of the first data word with the first set of one or more bytes of the second data word in response to the alignment signal (see lines 40-67 of column 10 and column 11 and lines 1-15 of column 12).

11. Referring to claims 33, Petersen discloses a method for performing fly-by read operation comprising:

reading the first data word from the memory device (see lines 45-67 of column 7, column 8, and lines 1-46 of column 9);

preloading the first data word into a read aligner; and then

reading a second data word from the first memory device (see lines 45-67 of column 7, column 8, and lines 1-46 of column 9);

applying a second data word to the read aligner (see lines 45-67 of column 7, column 8, and lines 1-46 of column 9);

creating a first fly-by read word routing a first portion of the first data word and a first portion of the second data word through the read aligner in response to the first alignment signal (see lines 45-67 of column 7, column 8, and lines 1-46 of column 9); and

transmitting the first fly-by read word on the system bus to a write aligner (see lines 45-67 of column 7, column 8, and lines 1-46 of column 9);

12. Referring to claims 34 and 35, Petersen teaches words will continue to be read and accumulated until enough valid data is available for a complete write transaction (see lines 45-67 of column 7, column 8, and lines 1-46 of column 9).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petersen (U.S. Patent No. 5,517,627) in view of Chauvel et al. (U.S. Patent No. 6,412,048 hereinafter "Chauvel").

15. Referring to claim 1, Petersen teaches a system comprising:

a system bus (see item labeled 14 in figure 7);

a direct memory access (DMA) controller coupled to the system bus (see item labeled 13 in figure 7);

a main memory (see item labeled 12 in figure 7); and a slave device coupled to the system bus and the DMA controller (see item labeled 15 in figure 7; Note the slave device is coupled to the DMA through the system bus), the slave device including a slave peripheral, a peripheral read aligner, a peripheral write aligner and a peripheral slave interface (see items labeled 15, 24, and 17, respectively).

Petersen fails to teach the system comprising a memory control device coupled to the system bus and the DMA controller, the memory control device including a memory controller, a

memory read aligner, a memory write aligner, and a memory slave interface.

Chauvel teaches a system comprising a memory control device coupled to the system bus and the DMA controller, the memory control device including a memory controller, a memory read aligner, a memory write aligner, and a memory slave interface (see item labeled 18 and the associated connections, and lines 29-59 of column 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Petersen with the teachings of Chauvel such that it comprises a memory control device coupled to the system bus and the DMA controller, the memory control device including a memory controller, a memory read aligner, a memory write aligner, and a memory slave interface in order to associate an initial priority value for a plurality of memory access requests as suggested by Chauvel (see lines 50-61 of column 3).

16. Referring to claim 2, Chauvel teaches the DMA controller us configured to implement fly-by read and fly-by write operations between the memory control device and the slave device (see lines 19-41 of column 5; Note Examiner is relying on applicant's

definition of fly-by transactions found in paragraph 2 of page 1 of the specification).

17. Referring to claims 3 and 5, Chauvel teaches the memory read aligner is configured to provide data words that are fully aligned with the system bus during fly-by write operations and that the memory write aligner is configured to process data words that are fully aligned with the system bus during fly-by read operations (see lines 29-59 of column 9).

18. Referring to claim 6, Chauvel teaches the memory write aligner is further configured to re-align the data words on the system bus to a byte address of the main memory during fly-by read operations (see lines 29-59 of column 9).

19. Referring to claims 4 and 7, Petersen teaches the peripheral read aligner is configured to provide data words that are fully aligned with the system bus during fly-by read operations (see lines 17-37 of column 12) and the peripheral write aligner is configured to process data words that are fully aligned with the system bus during fly-by write operations (see lines 40-55 of column 10).

20. Referring to claim 8, Petersen teaches the peripheral write aligner is further configured to re-align the data words on the system bus to a byte address of the slave peripheral during fly-by write operations (see lines 40-55 of column 10).

21. Referring to claim 9, Petersen discloses the slave peripheral includes a FIFO memory coupled to the peripheral read aligner and the peripheral write aligner (see lines 11-19 of column 10).

22. Referring to claim 10, Petersen discloses the slave device comprises means for adjusting a read pointer of the FIFO memory after a fly-by read operation (see lines 12-13 of column 13 and lines 47-50 of column 13).

23. Referring to claim 11, Petersen teaches the slave peripheral further comprises means for informing the peripheral read aligner and the peripheral write aligner of an alignment offset between the system bus and the FIFO memory (see item labeled 103 in figure 10 and item labeled 143 in figure 13).

24. Referring to claim 12, Petersen discloses each of the aligners include:

a barrel shifter coupled to receive a data word, a byte enable value and an alignment signal (see item labeled 60 in figure 9 and the associated connections);

a register coupled to receiver a data word and a byte enable value provided by barrel shifter (see items labeled 61-0 through 61-2 in figure 9)

an output multiplexer coupled to receive the data words and byte enable values provided by the barrel shifter and the register, the output multiplexer being controlled by the alignment signal (see items labeled 62-0 through 62-2 in figure 9).

25. Referring to claim 13, Petersen teaches each register includes:

a data register for storing a data word provided by the barrel shifter (see items labeled 61-0 through 61-2 in figure 9);

a byte enable register for storing a byte enable value provided by the barrel shifter (see 40-46 of column 5);

means for clearing the byte enable register (Note the byte enable value can be 1 or 0).

26. Referring to claim 14, Petersen discloses the aligner further includes:

means for preloading the register with a data word and byte enable value provided by the barrel shifter (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5);

means for loading the register with a data word and byte enable value provided by the barrel shifter (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5);

means for preserving a data word and a byte enable value in the register (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5); and

means for bypassing the barrel shifter in the register (see lines table 1 in column 5 and lines 43-67 of column 4 and lines 17-25 of column 5).

27. Claims 31 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petersen in view of Yarch et al. (U.S. Patent No. 5,761,532 hereinafter "Yarch").

28. Referring to claims 31 and 36, Petersen fails to teach the method including providing a ready signal on the system bus when

the memory device is in a ready state and providing a wait state when the memory device is in a wait state.

Yarch teaches, in an analogous system, a method including providing a ready signal on the system bus when the memory device is in a ready state and providing a wait state when the memory device is in a wait state (see lines 8-17 of column 3).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the method of method of Petersen with the teachings of Yarch such that it includes providing a ready signal on the system bus when the memory device is in a ready state and providing a wait state when the memory device is in a wait state. One of ordinary skill in the art would have been motivated to make such modification in order to prevent the loss of data from writing to the memory when it is not yet available.

Allowable Subject Matter

29. Claims 17-22 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

The following references are cited to further show the state of the art as it pertains to data alignment:

U.S. Patent No. 6,003,122 to Yarch et al.

U.S. Patent No. 5,737,761 to Holland et al.

U.S. Patent No. 6,055,761 to Bridges et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J Sorrell whose telephone number is 703 305-7800. The examiner can normally be reached on Monday-Friday 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

EJS
September 16, 2003

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100